

Figure 1

(Figures)

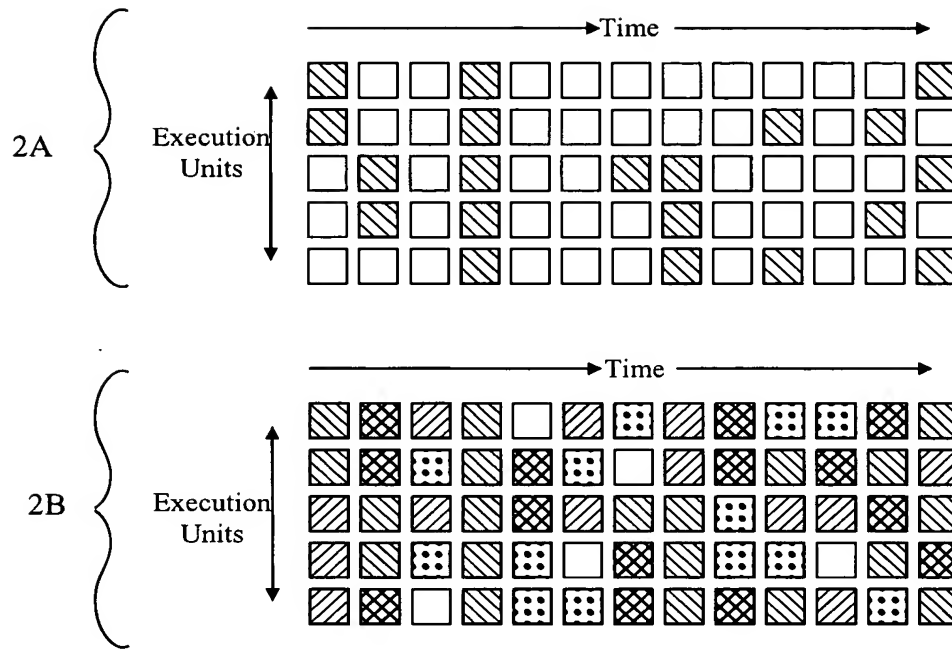


Figure 2

(Figures)

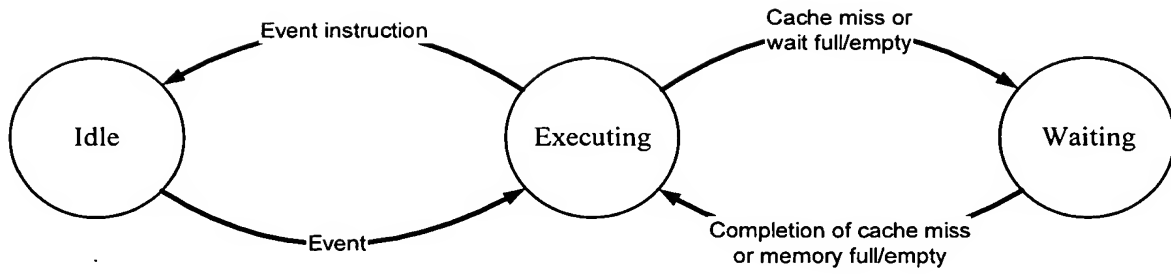


Figure 3

(Figures)



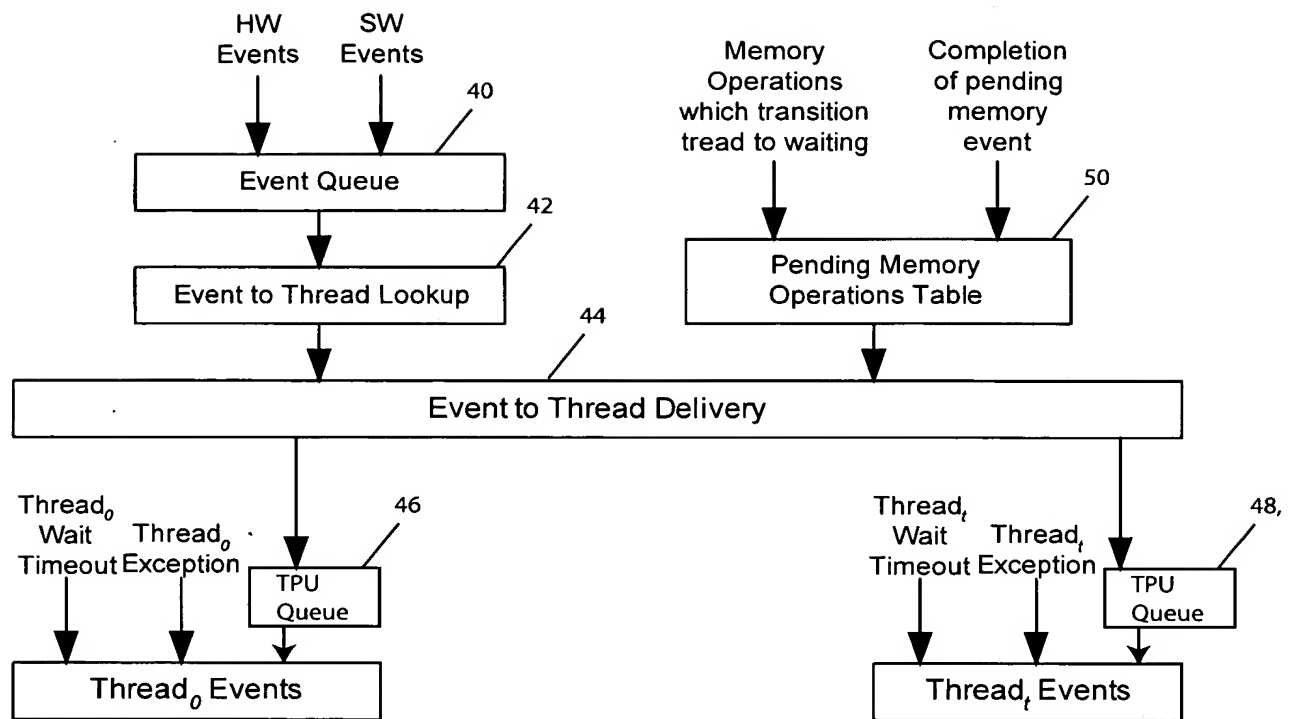


Figure 4

(Figures)



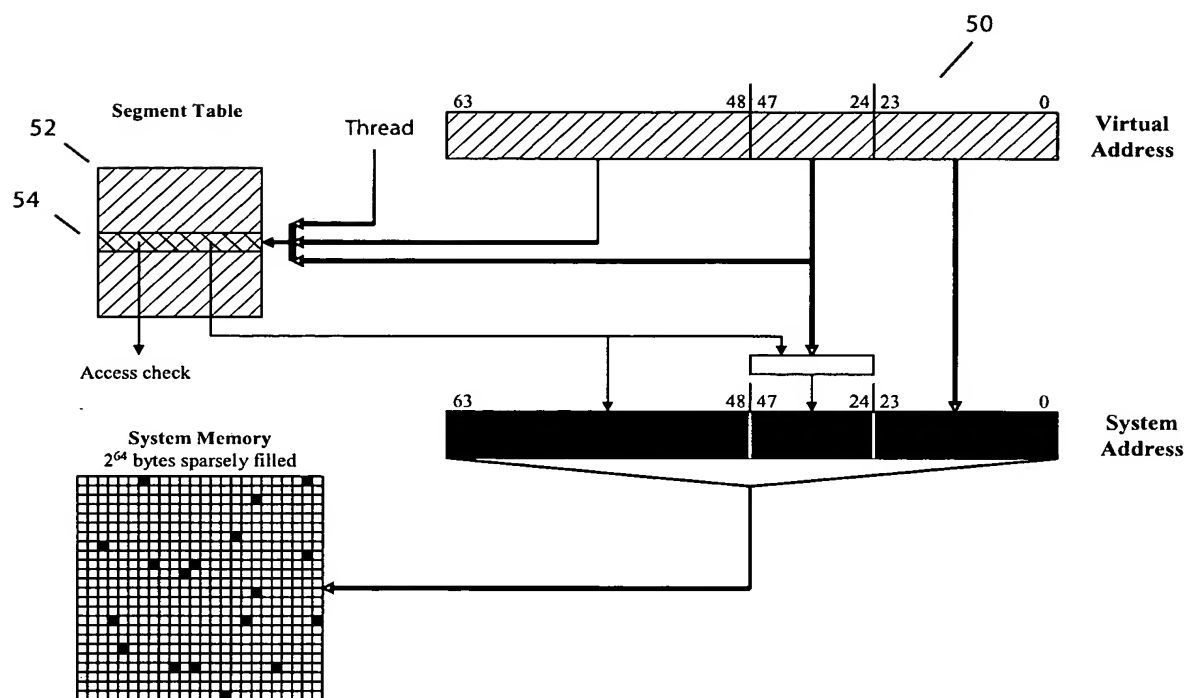


Figure 5

(Figures)

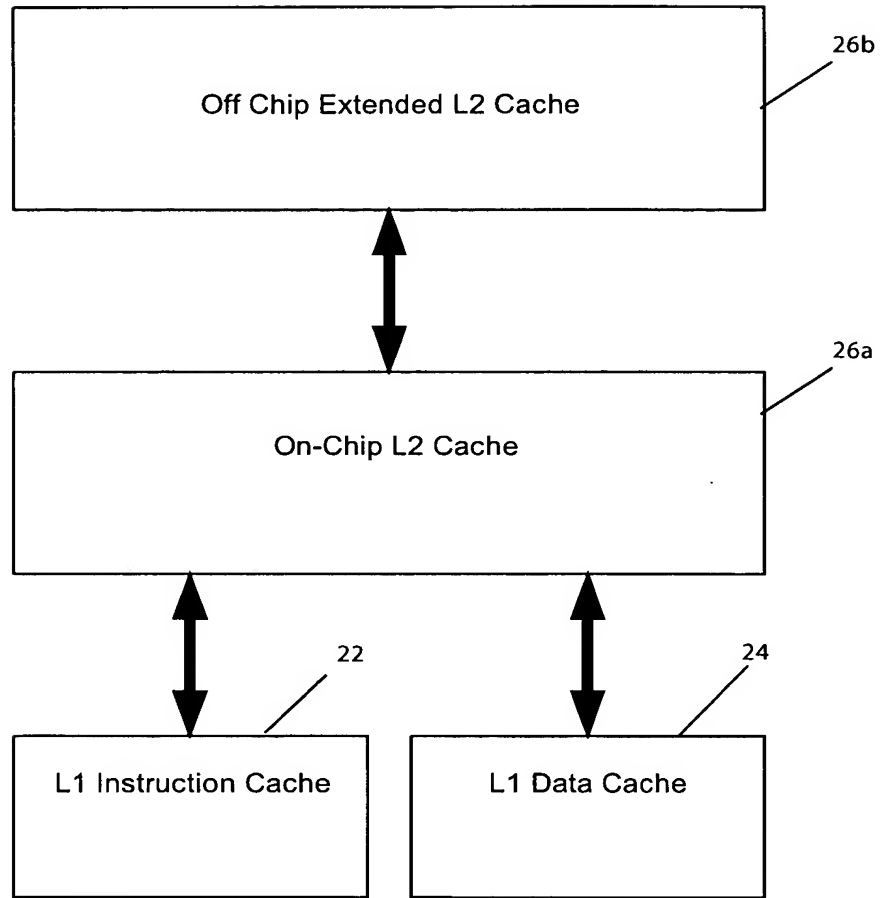


Figure 6

(Figures)





Sheet #7 of 26

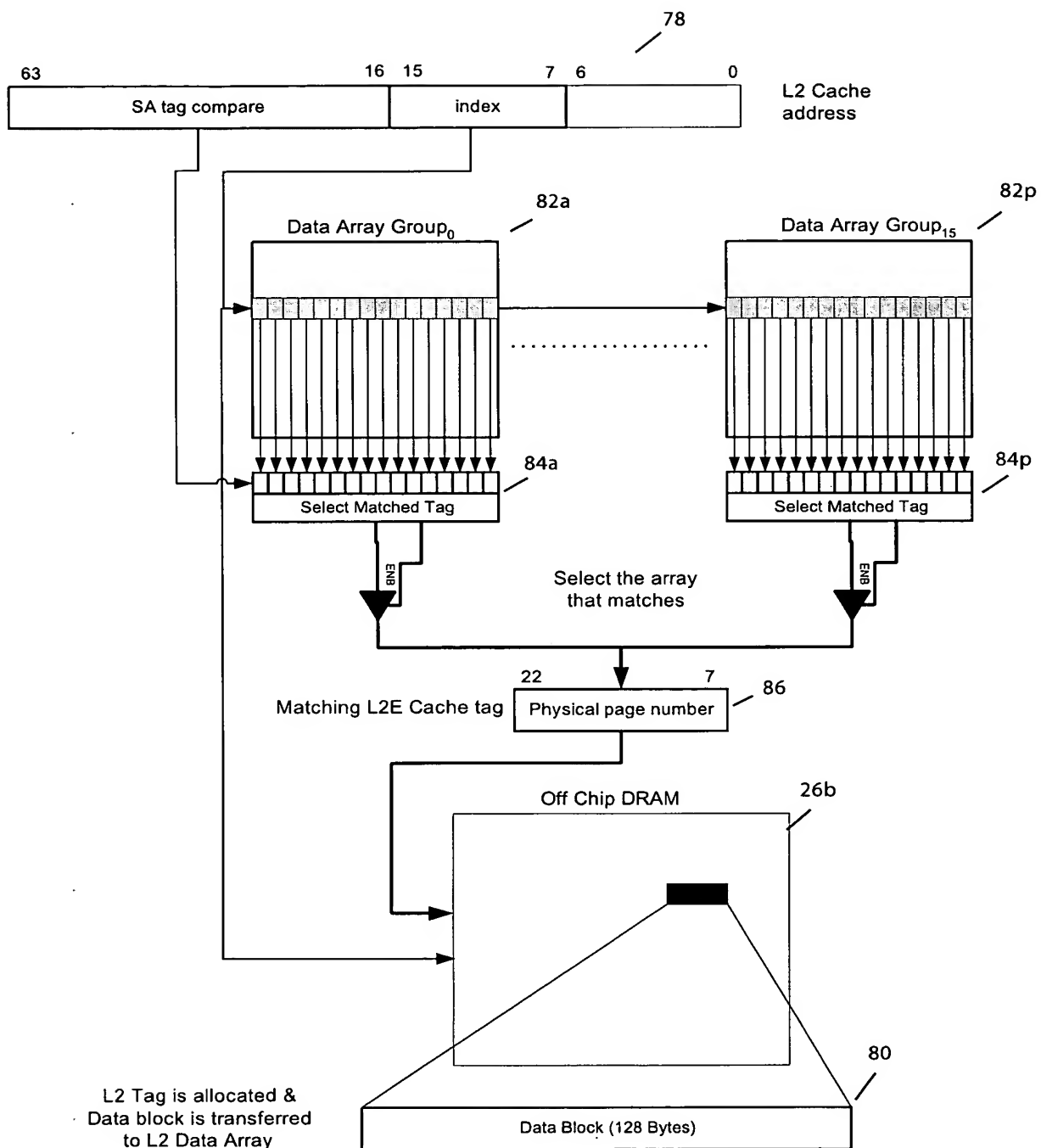
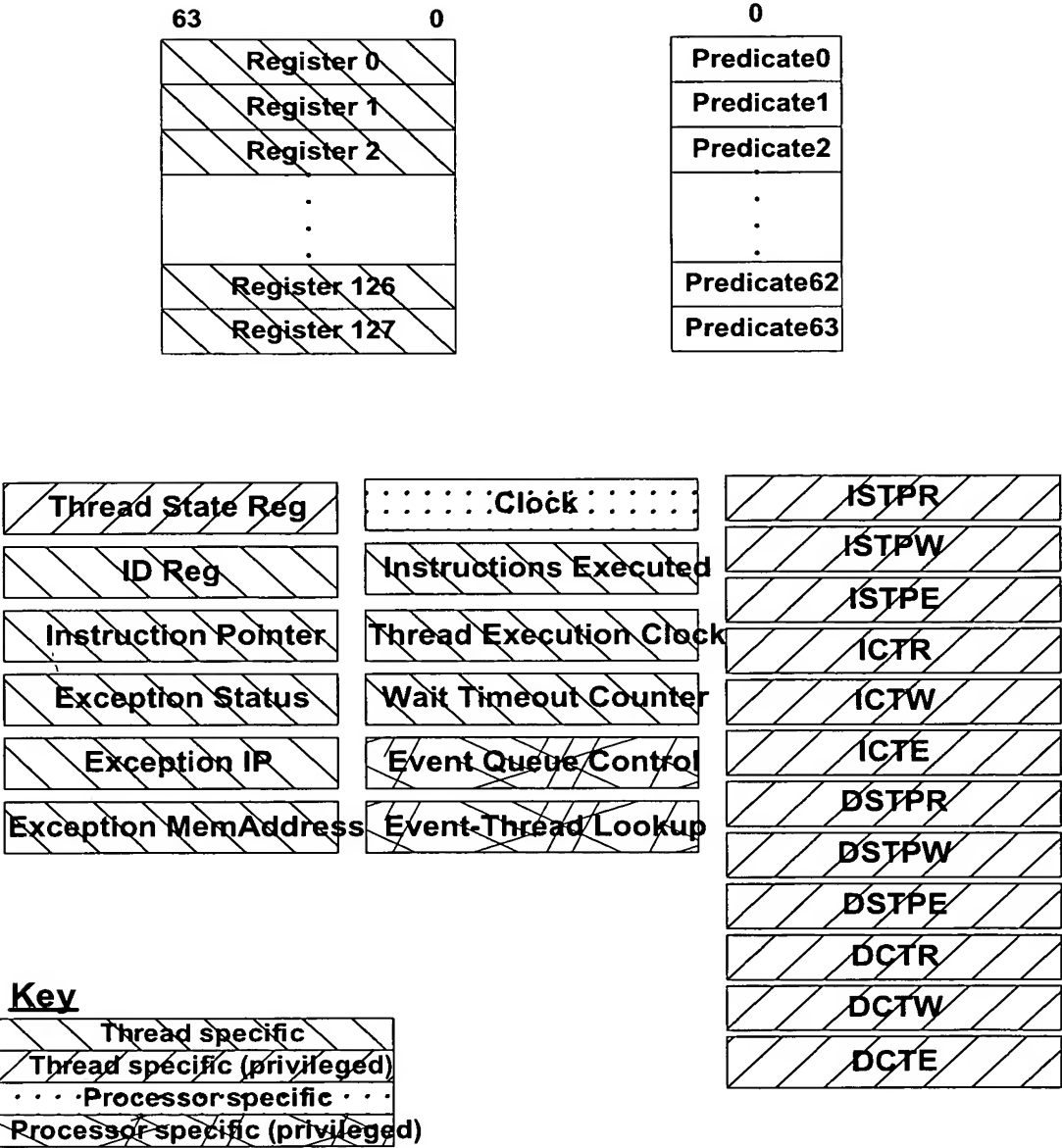


Figure 8

(Figures)



General Purpose Register File
TPU State Control Registers

Figure 9

(Figures)



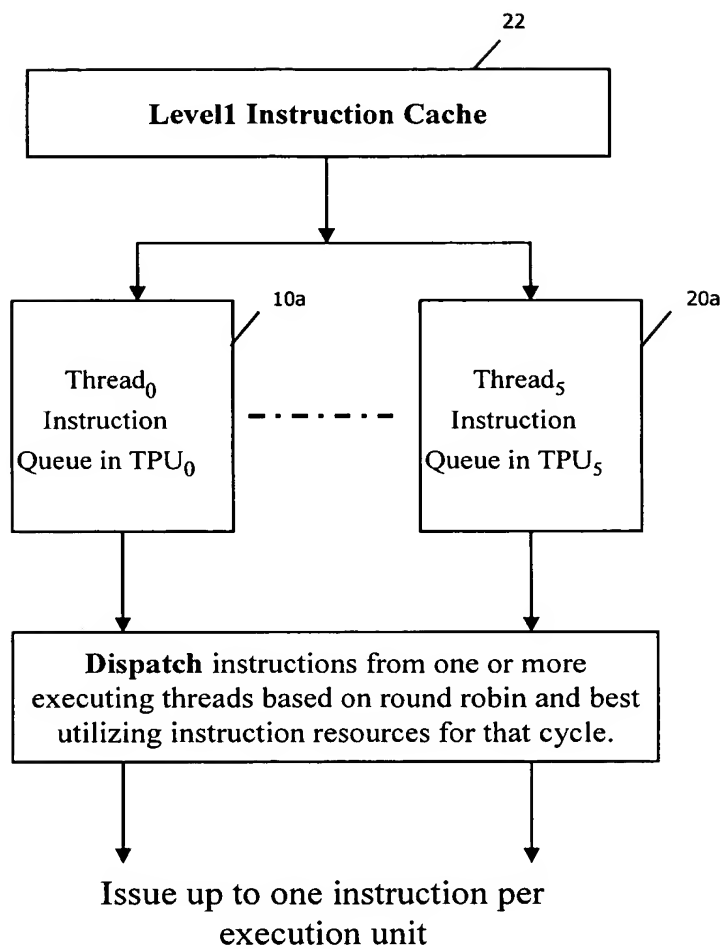


Figure 10

(Figures)

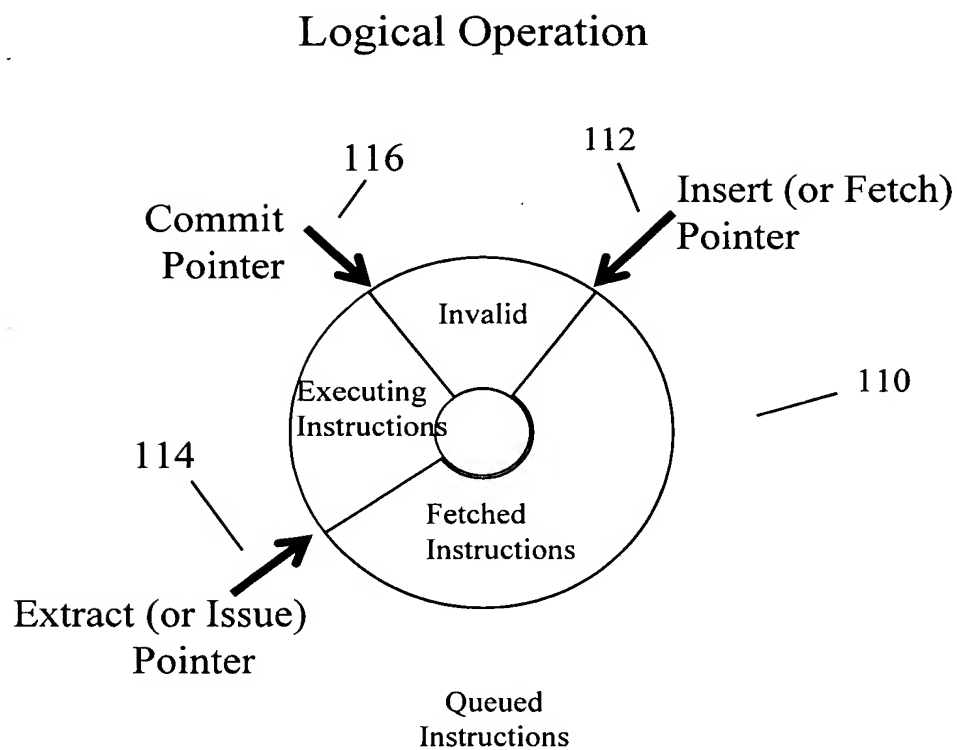


Figure 11

(Figures)

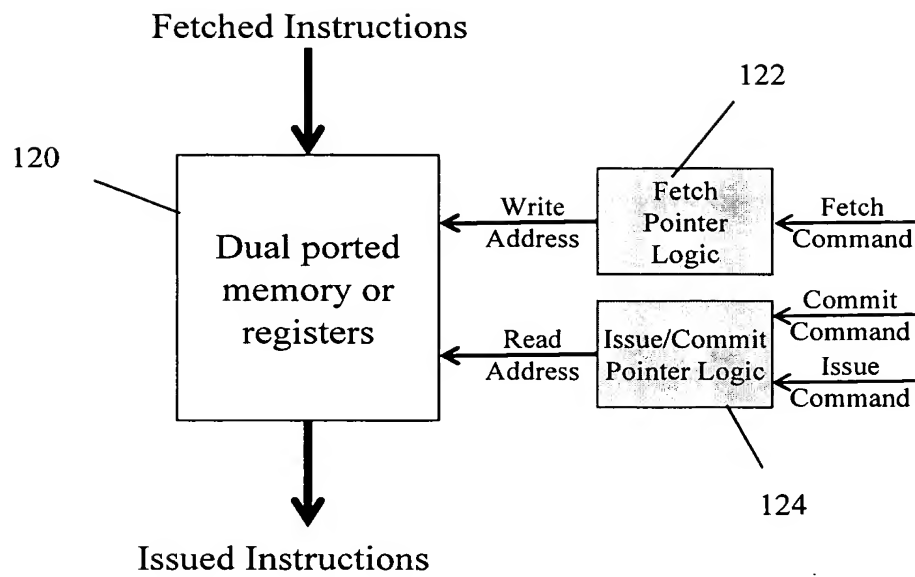


Figure 12

(Figures)

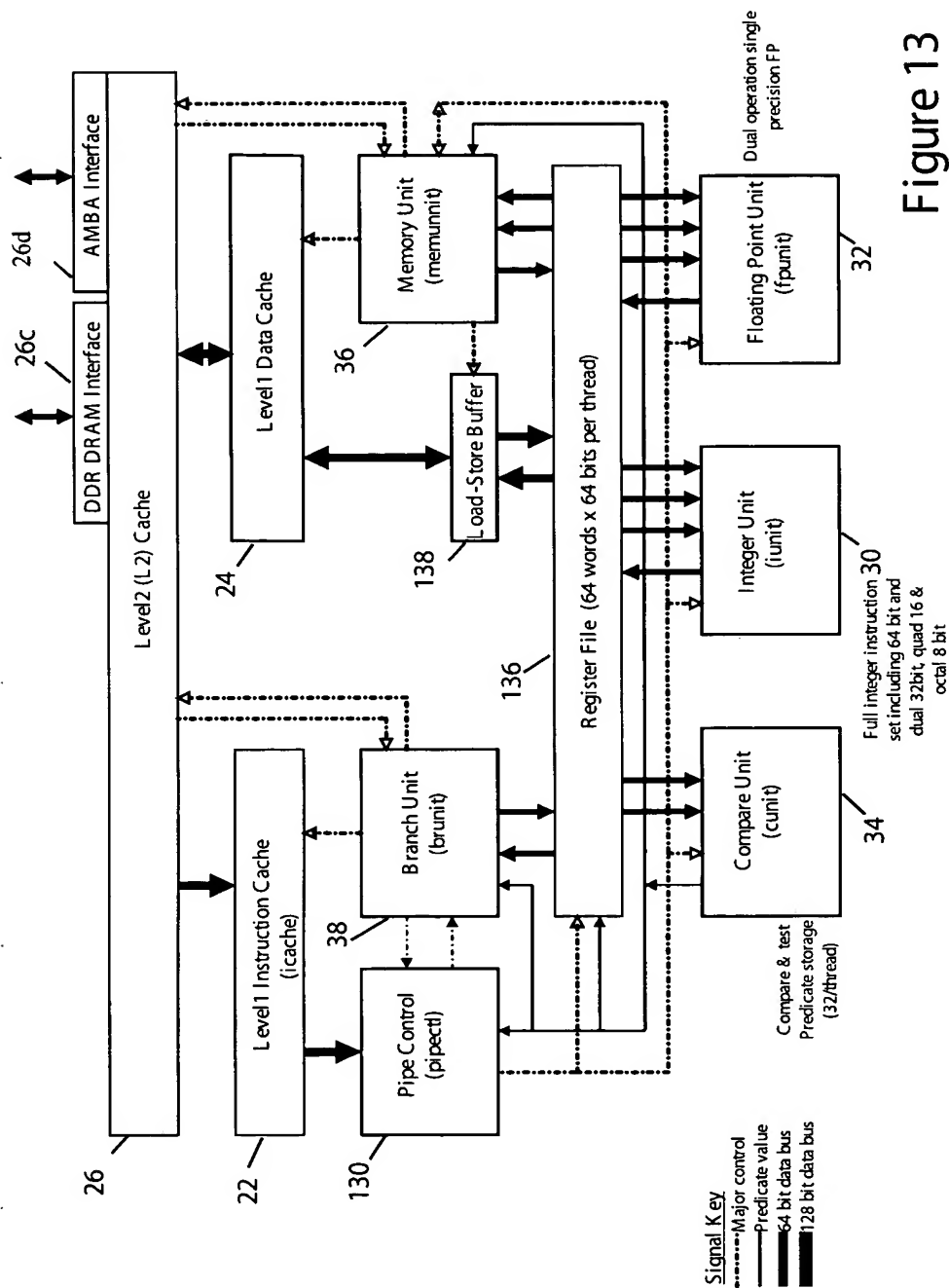


Figure 13

(Figures)

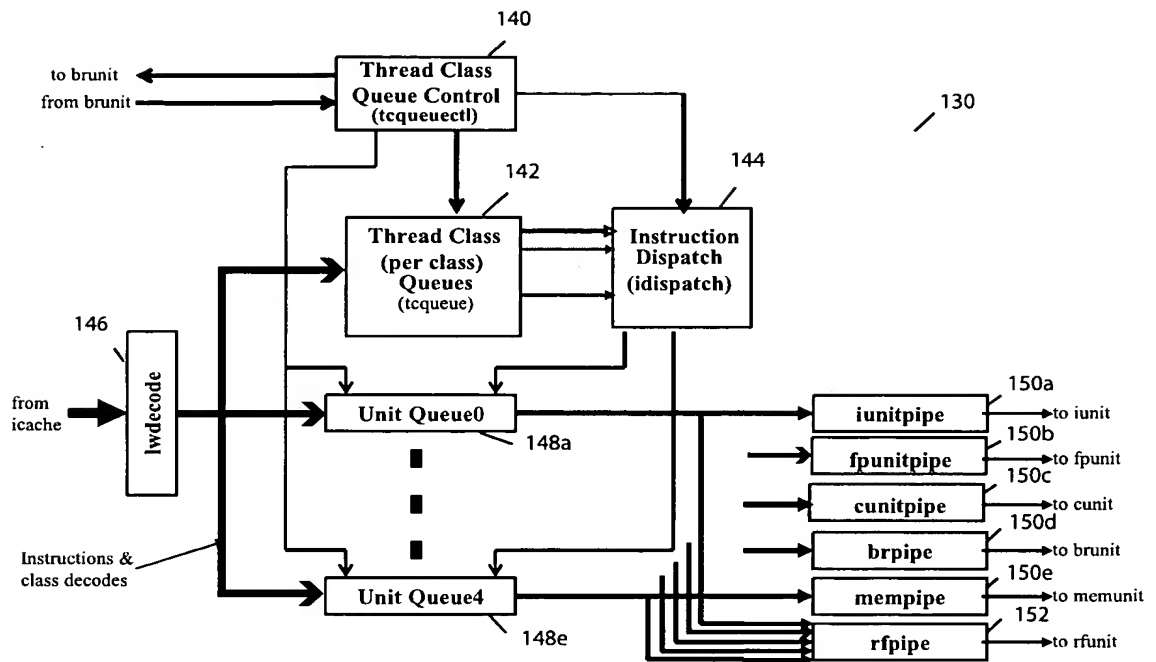


Figure 14

(Figures)

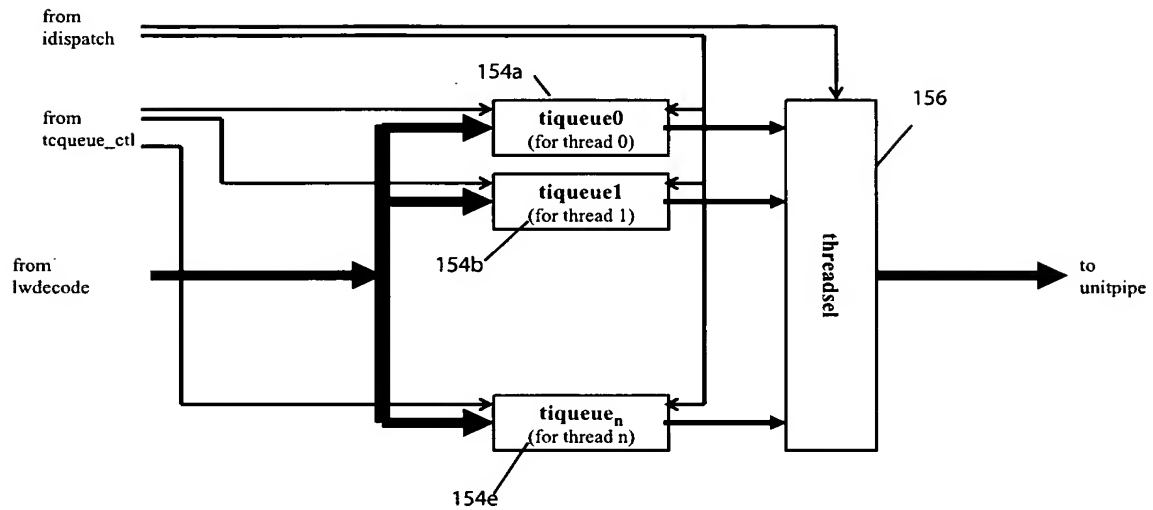


Figure 15

(Figures)

38

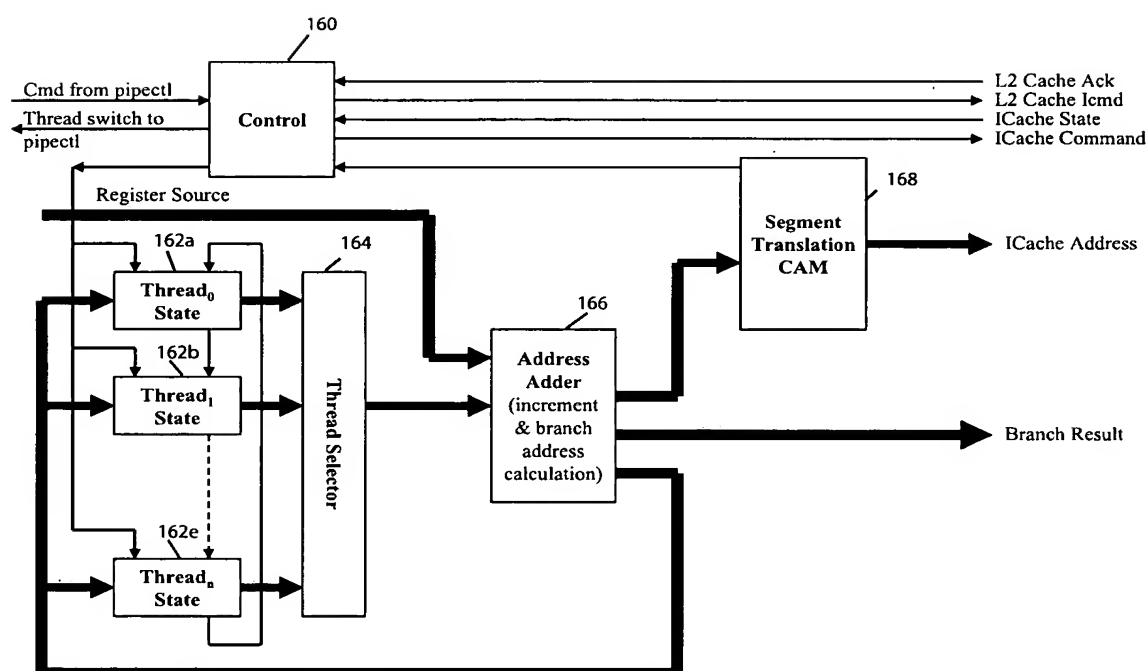


Figure 16

(Figures)

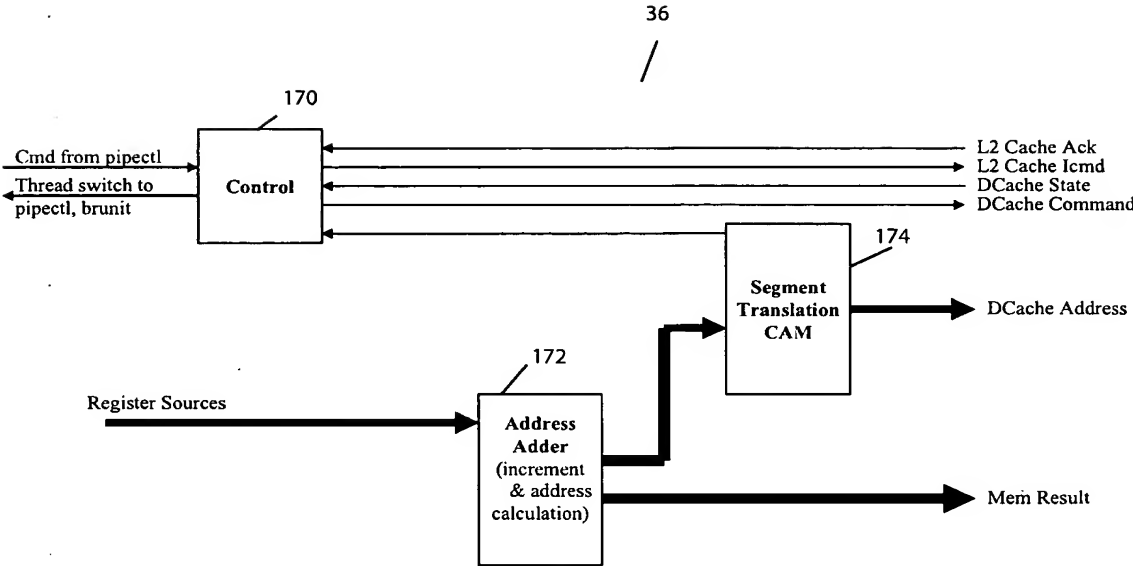


Figure 17

(Figures)

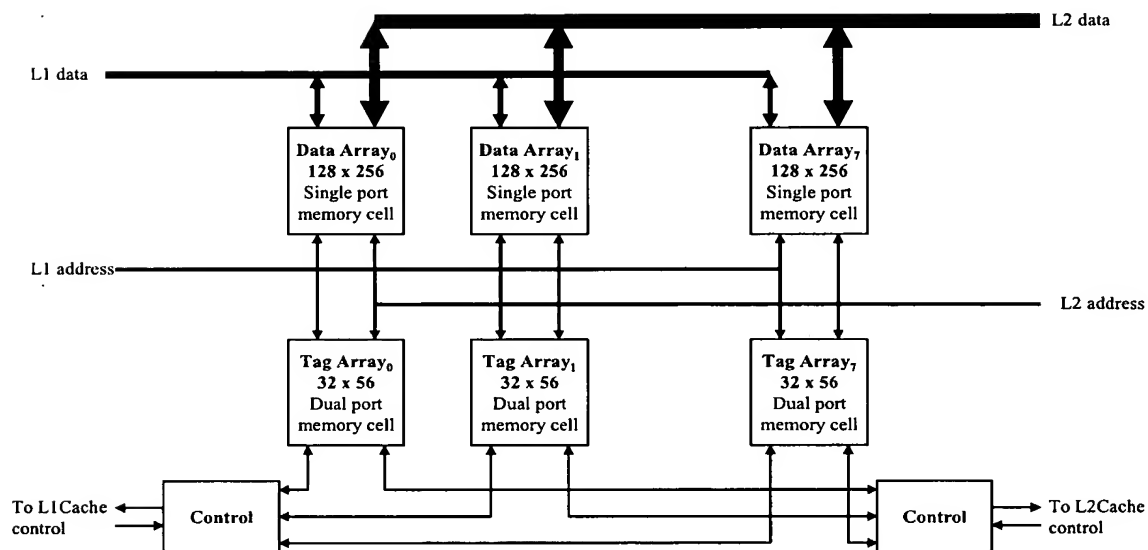


Figure 18

(Figures)

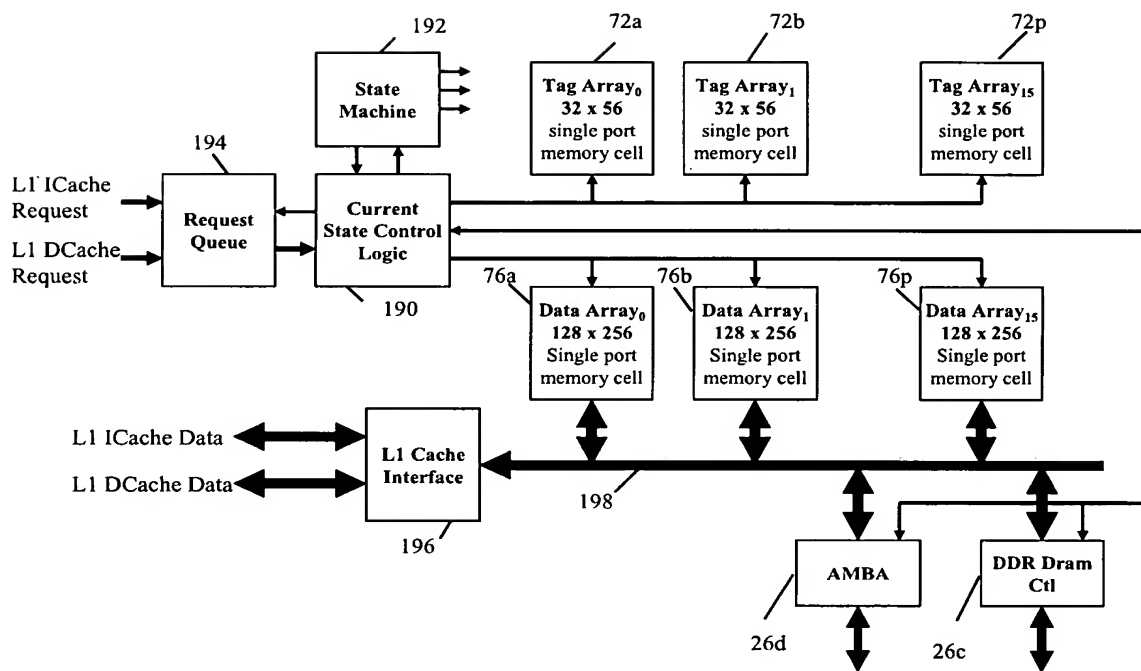


Figure 19

(Figures)

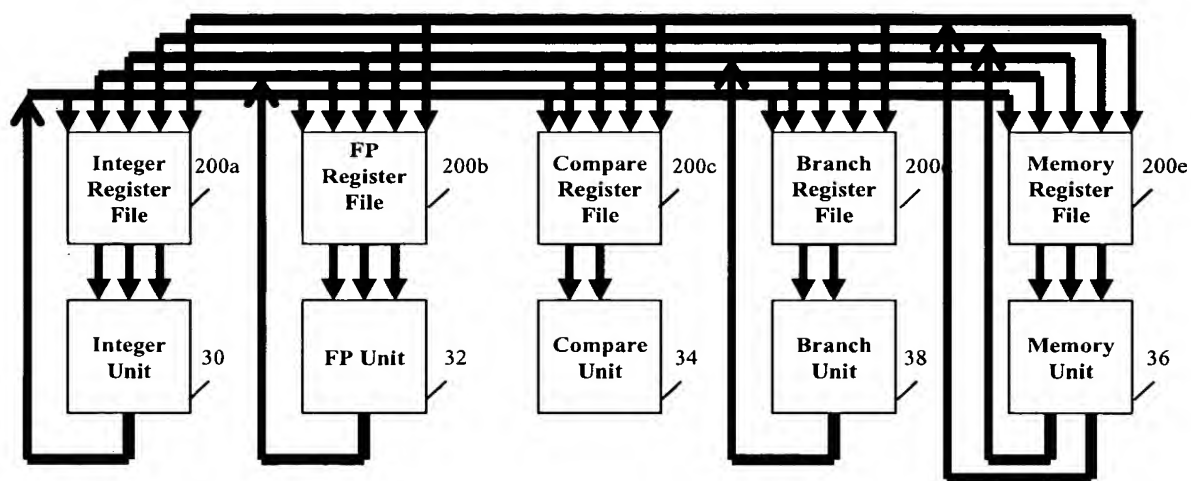


Figure 20

(Figures)

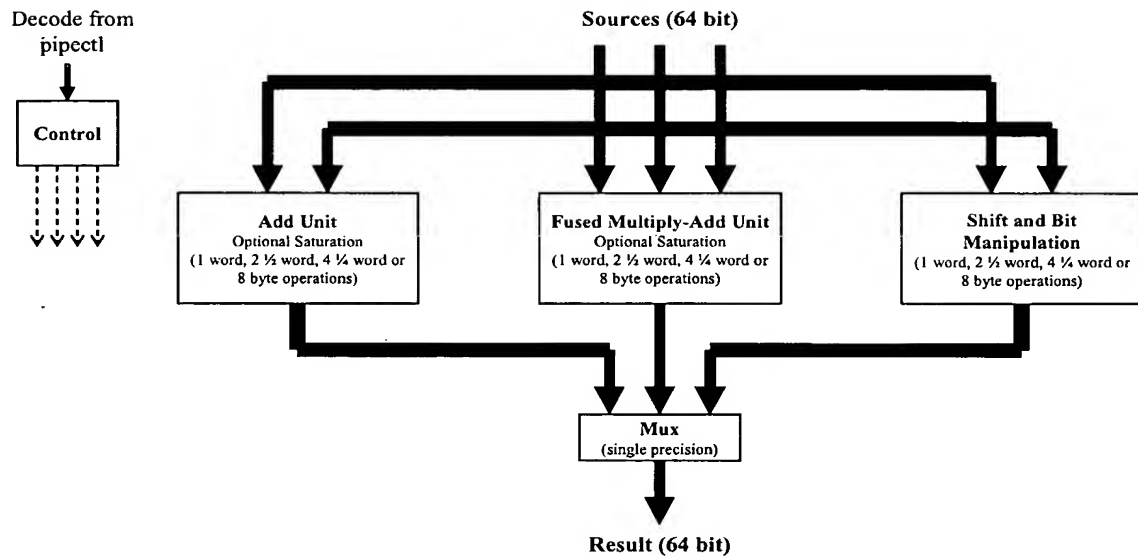


Figure 21

(Figures)

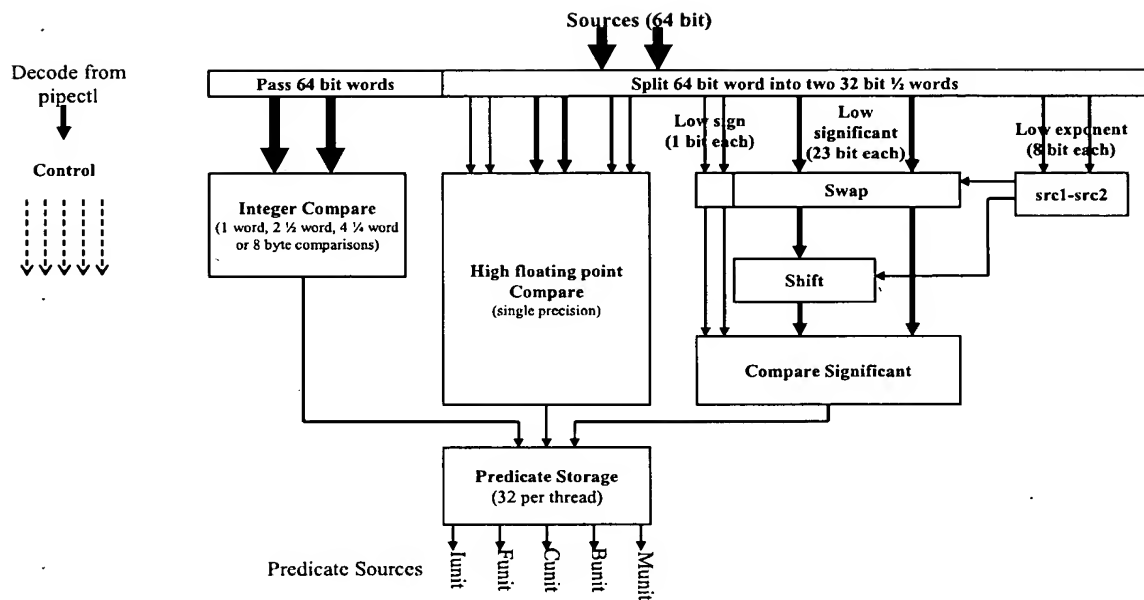


Figure 22

(Figures)

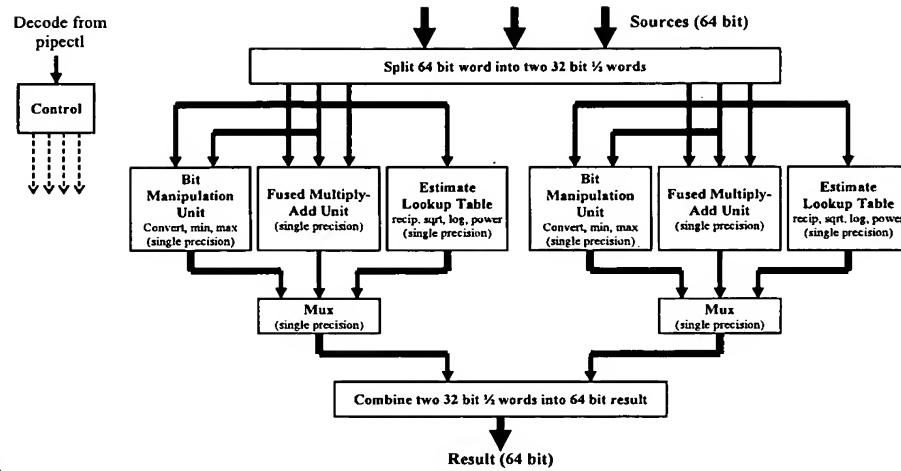


Figure 23A

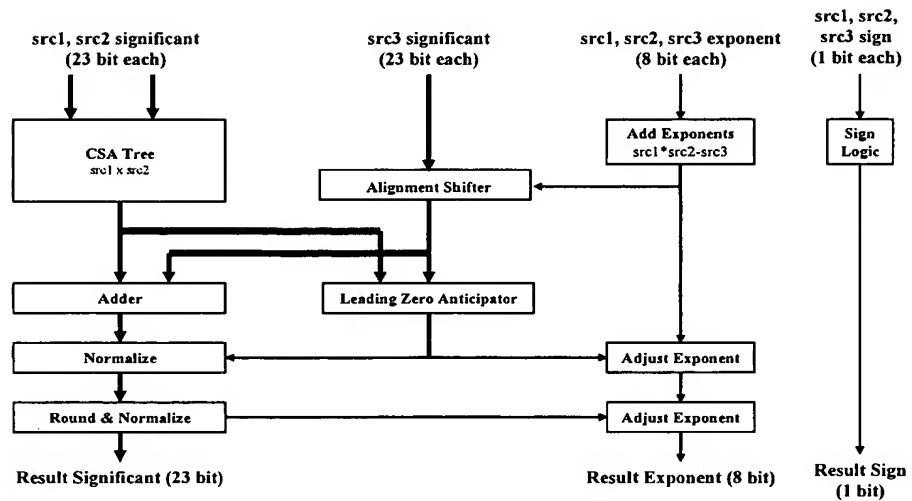


Figure 23B

(Figures)

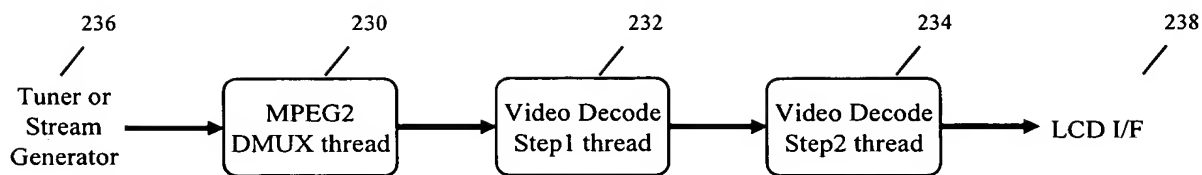


Figure 24A

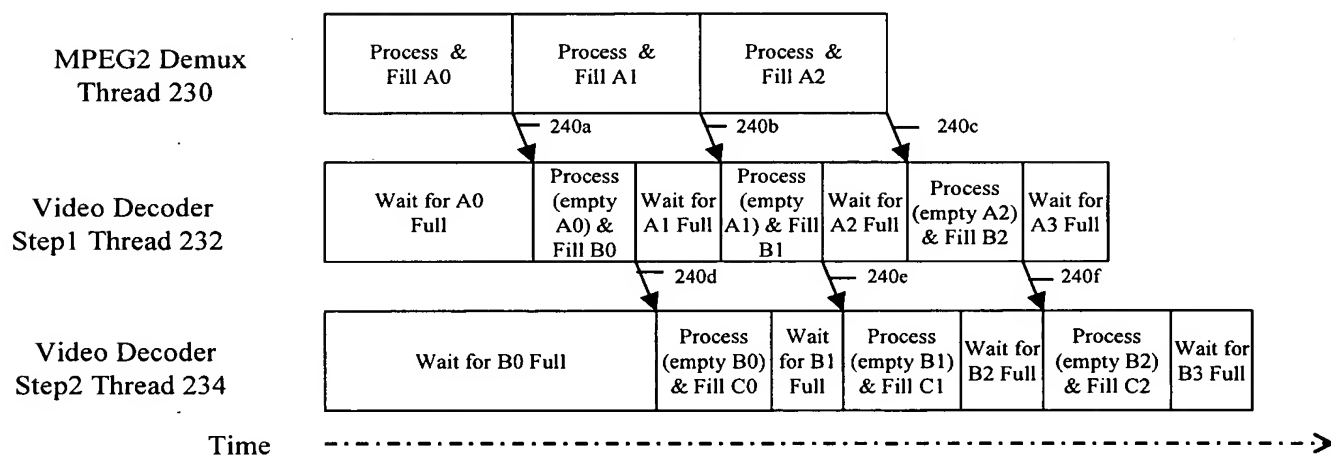


Figure 24B

(Figures)

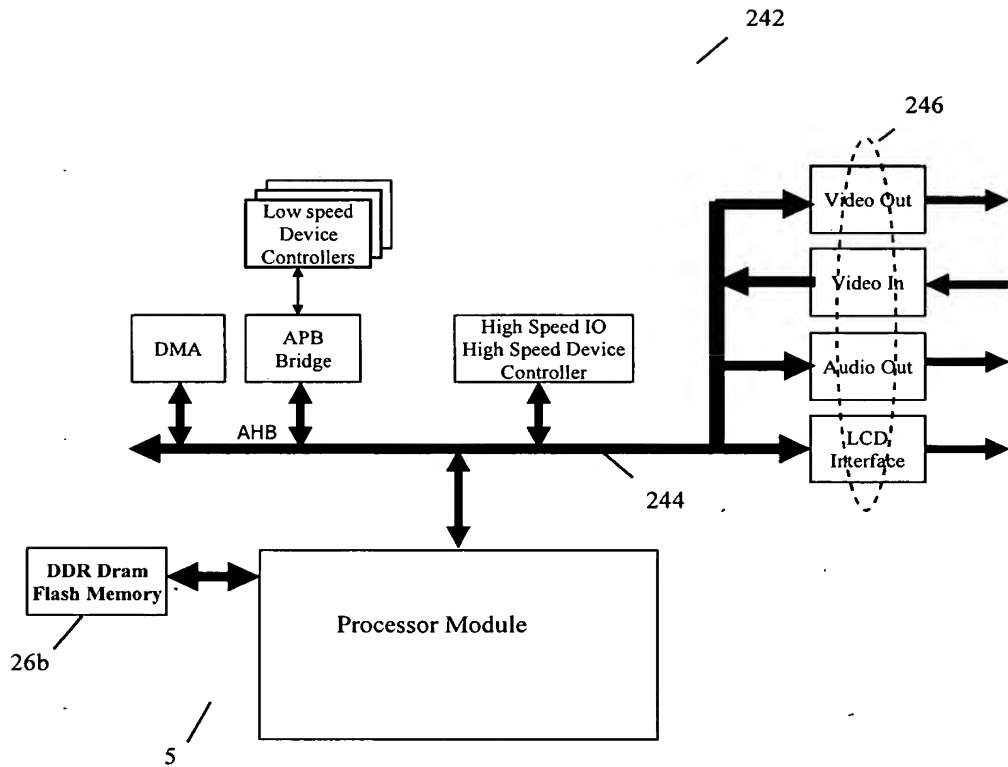


Figure 25

(Figures)

SOC Block Diagram

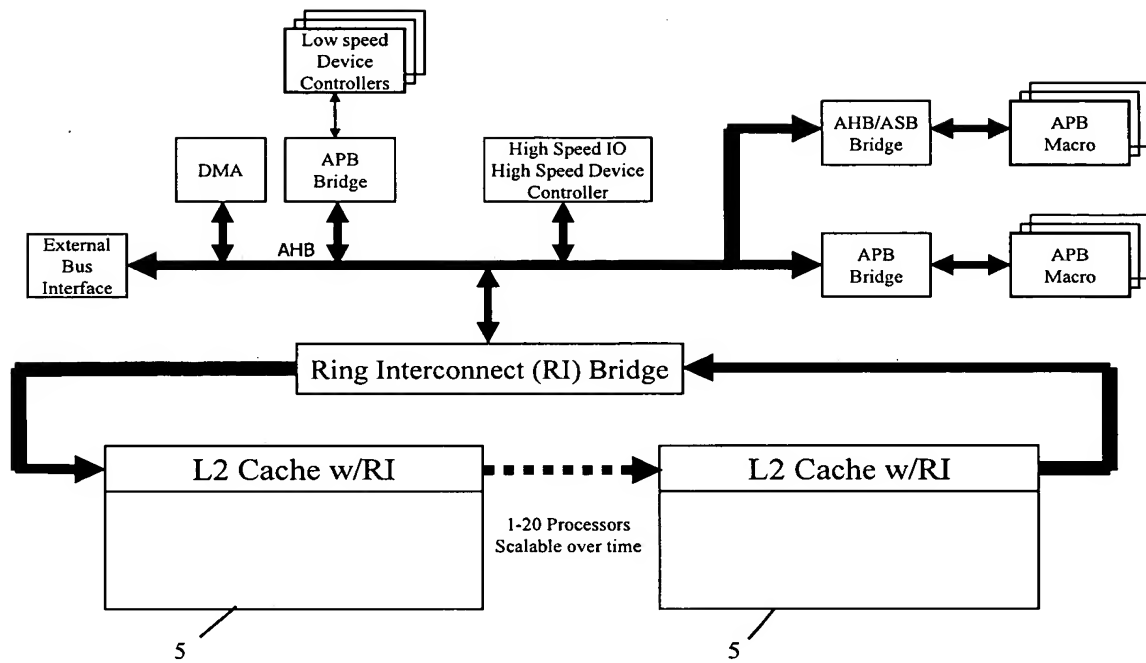


Figure 26

(Figures)